REMARKS

Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

In the Office Action dated January 30, 2002, the Examiner rejected Claims 1-4 and 7-11, 16 and 17 under 35 U.S.C. 102(e) as being anticipated by Ma et al. This rejection is respectfully traversed.

Applicant has amended the claims to distinguish the invention from the Ma et al. reference. In particular, Applicant has amended the claims to recite that a low resistance layer having broad area is disposed just under the signal input pad. This low resistance layer functions as a shield.

Applicant submits that Ma fails to disclose a semiconductor device with a first interconnection connected to a gate of the MOSFET, wherein said first interconnection constitutes a signal input pad for receiving an input signal for the MOSFET; a high concentration impurity diffused region located under the first interconnection and at a surface part of the semiconductor substrate; a second interconnection connected to the high concentration impurity diffused region; and a low resistance layer having broad area is disposed just under the signal input pad in order to function as a shield, as recited in Claims 1 and 7.

Ma discloses, for example, in Fig. 8, that the first interconnection 133 connects to a gate 55 and the second interconnection 135 connects between one electrode of the DPC (double polysilicon capacitor) 89 and the highly concentrated impurity diffused region 89 (substrate). At col. 8, lines 21-22, Ma discloses that the metallization region 133 (first interconnection) is electrically coupled to gate electrode 105. With respect to the Examiner's contention that elements 135, 89, and 99 of Ma meet Applicant's claimed features, this is in error. Elements 135, 89, and 99 are disclosed as portions of the DPC 57, not the IGFET 115.

Therefore, Ma does not disclose the claimed semiconductor device with the following spatial relations as recited in claims 1 and 7 (and claims 2-4, 6, 8-11, 13, 16, and 17 by virtue of dependency): the first interconnection 115, which constitutes a signal input pad 116 for receiving an input signal, is connected to a gate 107 of the MOSFET; the high concentration impurity diffused region 112 is disposed under the first interconnection 115; the second interconnection 117 is connected to the high concentration impurity diffused region 121; the gate 107 and the high concentration impurity region 121 are not connected because their functions are different. The features of the present invention provide the high concentration

impurity diffused region for eliminating any substrate potential. This region is disposed beneath the signal input interconnection, and is connected to the gate of the MOSFET device.

Applicant respectfully submits that claims 1 and 7 (and claims 2-4, 8-11, 16, and 17 by virtue of dependency) are not anticipated by Ma, and are also allowable.

In addition, the Examiner rejected claims 6 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Ma et al.as applied to claims 1-4, 7-11, 16 and 17 above, and further in view of Battersby et al. U.S. Patent No. 5,528,065. This rejection is respectfully traversed.

As set forth above, in the Ma et al. reference, there is neither disclosed nor suggested that such low resistance layer is disposed just under the signal input pad. Furthermore, there is no description of a signal input pad and its shape and location.

Since Ma et al. do not disclose essential features of the present invention as recited in amended independent Claims 1 and 7, and by the virtue of the dependency Claims 6 and 13 therefrom, Applicant submits that because the main claims have been amended, the Examiner's statements about dependent claims are now of no meaning. Further, the alleged combination of Ma et al. and Battersby et al. would not result in the claimed invention because there is no guidance or motivation found in either Ma et al. or Battersby et al. that would obviously lead one of ordinary skill to the recited claim limitations. Consequently, Applicant submits that Claims 1-4, 6, 7-11, 13, and 16-19 are allowable over the cited prior art references.

In view of the foregoing, the claims are now believed to be in form for allowance, and such action is hereby solicited. If any point remains in issue which the Examiner feels may be best resolved through a personal or telephone interview, please contact the undersigned at the telephone number listed below.

Attached is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed on the substrate;

a [first interconnection] signal input pad connected to a gate of the MOSFET, [wherein said first interconnection constitutes a] said signal input pad [for] receiving an input signal for the MOSFET;

a high concentration impurity diffused region located just under the [first interconnection] signal input pad and at a surface part of the semiconductor substrate;

[a second] an interconnection connected to the high concentration impurity diffused region, said interconnection being electrically isolated from said signal input pad; and

a low resistance layer provided on the upper surface of the high concentration impurity diffused region.

7. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOSFET formed on the substrate;

a [first interconnection] signal input pad connected to a gate of the MOSFET, [wherein said first interconnection constitutes a] said signal input pad [for] receiving an input signal for the MOSFET;

a high concentration impurity diffused region located below the [first interconnection] signal input pad and at a surface part of the semiconductor substrate;

[a second] an interconnection connected to the high concentration impurity diffused region, said interconnection being electrically isolated from said signal input pad;

[a low resistance layer provided on the upper surface of the high concentration impurity diffused region; and]

a polysilicon layer provided [below the first interconnection] just under said signal input pad, said polysilicon layer being connected to the [second] interconnection, and

a low resistance layer provided on the upper surface of the high concentration impurity diffused region and said polysilicon layer.

The following new claims have been added.

18. (New) The semiconductor device according to claim 1, wherein said signal input pad locates within an area of the high concentration impurity diffused region.

19. (New) The seminconductor device according to claim 7, wherein said signal input pad locates within an area of the polysilicon layer.

END OF APPENDIX